Image BAF/2811

TRANSMITTAL LETTER			Case No. 10519-57
Serial No. 09/928,975	Filing Date August 13, 2001	Examiner T. Magee	Group Art Unit 2811
Inventor(s) Herner et al.			
Title of Invention LOW RESISTIVITY TITANIUM SILICIDE ON HEAVILY DOPED SEMICONDUCTOR			

TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is Transmittal Letter (in duplicate); Appeal Brief (17 pages in triplicate); and Postcard Receipt.

☐ Small entity status of this application under 37 CFR § 1.27 has been established by verified statement previously submitted.

☐ A verified statement to establish small entity status under 37 CFR §§ 1.9 and 1.27 is enclosed.

☐ Petition for a _month extension of time.

☐ No additional fee is required.

☐ The fee has been calculated as shown below:

	Claims Remaining After Amendment		Highest No. Previously Paid For	Present Extra	Small Entity Rate	Small Entity Add'l Fee	or	Other Than Small Entity Rate	Other Than Small Entity Add'l Fee
Total		Minus			x $9=			x $18=	
Indep.		Minus			x 43=			x $86=	
First Presentation of Multiple Dep. Claim					+$145=			+ $290=	
					Total add'l fee	$		Total add'l fee	$

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☒ The Commissioner is hereby authorized to charge payment of any additional filing fees required under 37 CFR § 1.16 and any patent application processing fees under 37 CFR § 1.17 associated with this communication or credit any overpayment to Deposit Account No. 23-1925. A duplicate copy of this sheet is enclosed.

☒ I hereby petition under 37 CFR § 1.136(a) for any extension of time required to ensure that this paper is timely filed. Please charge any associated fees which have not otherwise been paid to Deposit Account No. 23-1925. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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Date: January 21, 2004 Signature:

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Name of Applicant, Assignee or Registered Representative

Signature

Our Case No. 10519-57

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		Group Art Unit: 2811
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APPEAL BRIEF

Commissioner for Patents
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V. Summary of Invention

Titanium silicide ($TiSi_2$) has been a commonly-used metallization in silicon integrated circuits. However, a problem occurs when commonly-used techniques are employed to fabricate $TiSi_2$. Specifically, as the line width of a structure is decreased below 0.3μm, it becomes more difficult to transform the relatively-high-resistivity C49 phase $TiSi_2$ into the relatively-low-resistivity C54 phase $TiSi_2$. This inability to obtain low resistivity $TiSi_2$ on small features has been called the "fine line effect."

Applicants invented a new "starting structure" for fabricating $TiSi_2$ to avoid the fine line effect (independent Claim 1). With reference to Figure 3, this "starting structure" comprises a first semiconductor region 12 characterized by a dopant concentration greater than $1x10^{19}/cm^3$ and a second semiconductor region 28 overlying the first semiconductor region 12. The second semiconductor region 28 comprises silicon and is characterized by a dopant concentration less

than $1x10^{19}/cm^3$ and a thickness t1. The structure also has a layer 30 comprising titanium directly overlying the second semiconductor region 28. (Page 4, line 18 – page 5, line 16). The layer 30 is characterized by a line width no greater than 0.3μm and a thickness t2, wherein $t1 > 1.2t2$. (Page 7, lines 25-31). The relationship between t1 and t2 is such that t1/t2 is sufficiently small that, when the layer 30 is reacted with the second semiconductor region 28 to form titanium disilicide 14 (see Figure 4), the titanium disilicide 14 is in ohmic contact with the first semiconductor region 12. As defined on page 7, lines 21-24, two layers are in "ohmic contact" when the curve of voltage versus current across the two layers is substantially linear over the range ± 5V, i.e., the maximum deviation of the slope of the voltage versus current curve from the average slope of the curve over the range ± 5V is ± 10% of the average slope. The relationship between t1 and t2 is such that t1/t2 is also sufficiently large that, when the layer 30 is reacted with the second semiconductor region 28 to form titanium disilicide 14, the titanium disilicide 14 anneals to a phase with a sheet resistance less than 3 ohms/square. (Page 6, lines 3-9).

While Claim 1 recites a "starting structure" for fabricating $TiSi_2$, independent Claim 7 recites a semiconductor structure that contains already-fabricated $TiSi_2$. With reference to Figure 1, this semiconductor structure comprise a first semiconductor region 12 characterized by a boron dopant concentration greater than $1x10^{20}/cm^3$ and a set of titanium silicide conductors 14, 22 directly overlying the first semiconductor region 12 and in ohmic contact therewith. Each conductor 14, 22 is characterized by a width no greater than 0.3μm, and at least 90% of the conductors 14, 22 are characterized by a sheet resistance less than 3 ohms/square. (Page 8, lines 1-6). The set of titanium silicide conductors 14, 22 is formed, in part, by a second semiconductor region 28 overlying the first semiconductor region 12, the second semiconductor region 28 comprising silicon and characterized by a dopant concentration less than $1x10^{18}/cm^3$ (see Figure

3). (Page 4, line 29 – page 5, line 6). The semiconductor structures described above can comprises a 3-D memory array comprising a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip. (Page 3, lines 16-20).

VI. Issues

There are three issues presented in this appeal:

1. Whether Claims 1-6 are unpatentable under 35 U.S.C. § 103(a) over the proposed combination of Hu et al.[1], Wilson et al.[2], Nakayama et al.[3], and Spinelli et al.[4];

2. Whether Claim 7 is unpatentable under 35 U.S.C. § 103(a) over the proposed combination of Hu et al., Wilson et al., Nakayama et al., and Spinelli et al.; and

3. Whether Claim 8 is unpatentable under 35 U.S.C. § 103(a) over the proposed combination of Hu et al., Wilson et al., Nakayama et al., Spinelli et al., and Tsukude et al.[5]

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[1] U.S. Patent Application No. US 2002/0045342A1.

[2] Wilson et al., "Handbook of Multilevel Metallization for Integrated Circuits," Noyes Publ., Westwood, New Jersey, pages 44-50 (1993).

[3] Nakayama et al., "Excellent Process Control Technology for Highly Manufacturable and High Performance 0.18 μm CMOS LSIs," IEEE Digest Tech. Papers, Symposium on VLSI Technology, pages 146-147 (1998).

[4] Spinelli et al., "An Improved Formula for the Determination of the Polysilicon Doping," IEEE Electron Device Letters, vol. 22, no. 6, pages 281-283 (June 2001).

[5] Tsukude et al., "A 256 Mb DRAM," Advance Magazine, Mitsubishi Electric, Vol. 75, pages 5-8 (June 1996).

VII. Grouping of Claims

Applicant identifies the grouping of the claims as follows:

Group I: Claims 1-6. Claims 1-6 do not stand or fall together.

Group II: Claim 7

Group III: Claim 8

VIII. Argument

A. Claim 1 Is Patentable over the Applied References

1. Introduction

Independent Claim 1 recites a semiconductor structure with first and second semiconductor regions and a titanium layer having a line width no greater than 0.3 μm. Claim 1 also recites a relationship between the thickness of the second semiconductor region and the titanium layer, such that when the titanium layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide is in ohmic contact with the first semiconductor region and anneals to a phase with a sheet resistance less than 3 ohms/square.

In the Office Action, several of the recited claim elements were asserted to be taught by Hu et al. (the primary reference in the 35 U.S.C. § 103(a) rejection), and other recited claim elements were admitted to be missing from Hu et al. Wilson et al., Nakayama et al., and Spinelli et al. were used as secondary references in an attempt to cure the admitted deficiencies. Applicants respectfully submit that independent Claim 1 is patentable over the proposed combination because (1) Hu et al. does not teach the elements asserted in the Office Action to be

present in Hu et al. and (2) the secondary references do not cure the admitted deficiencies in Hu et al.[6]

2. Hu et al. Does Not Teach the Elements Asserted in the Office Action to Be Present in Hu et al.

In the Office Action, it was asserted that element 218 in Figure 2E of Hu et al. is a titanium layer having a line width of less than 0.25 microns. Applicants respectfully disagree. As stated at paragraph 0026 (page 3), element 218 is a conductor layer of tungsten or ***titanium silicide*** *— **not titanium***. Accordingly, element 218 does not correspond to the layer of titanium recited in Claim 1. Further, the calculated thicknesses in the Office Action were based on the tungsten or titanium silicide layer and do not relate to a thickness of a titanium layer. Accordingly, Hu et al. also fails to disclose the thickness relationship recite in Claim 1.

Additionally, there is no teaching in Hu et al. that element 218 has a line width of less than 0.25 microns, as asserted in the Office Action. There are two disclosed embodiments in Hu et al. One embodiment lowers resistivity by forming a diffusion barrier using oxygen or nitrogen in a word line stack to prevent diffusion from a bottom silicon layer to a conductor layer. ***There is no disclosure in this embodiment of line widths less than 0.3 μm.*** In the second embodiment, barrier elements are used to form a low-dose matrix in silicon to modify the grain size in the conductor layer in order to lower resistivity. It is this embodiment — not the first embodiment — that relates to sub-0.3 micon word lines. However, Figure 2 and the sections of Hu et al. relied upon in the Office Action for the teaching of the titanium layer relate to the first embodiment, which does not teach line widths no greater than 0.3 μm. Accordingly, even if

[6] In the Office Action, the Examiner noted that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. Applicants agree; however, Applicants are not attacking the references individually. The discussion of individual references is presented to show that, *when the references are combined*, the combination *as a whole* fails to teach each and every claim element.

element 218 were a titanium layer, which it is not, Hu et al. would still be deficient because there is no teaching that element 218 has a line width no greater than 0.3 μm, as recited in Claim 1.

Additionally, in the embodiment that relates to sub-0.25 micon word lines, there is no teaching of the semiconductor structure recited in Claim 1. Hu et al. provides a low resistivity, sub-0.25 micon word-line titanium disilicide device by using a semiconductor structure that is different from the one recited in Claim 1. Whereas the semiconductor structure in Claim 1 has a specific thickness relationship between the titanium layer and the second semiconductor region, the semiconductor structure used in Hu et al. does not. Instead, the semiconductor structure used in Hu et al. has barrier elements that form a low-dose matrix in silicon to modify the grain size in the conductor layer. Accordingly, Hu et al. teaches a different semiconductor structure than the one recited in Claim 1.

In summary, because Hu et al. fails to disclose the claim elements asserted to be taught by Hu et al., the foundation of the rejection is fatally flawed. Because the secondary references do not cure this deficiency (or the additional deficiencies admitted by the Examiner), Applicants respectfully submit that Claim 1 is patentable over the proposed combination.[7]

3. The Secondary References Do Not Cure the Admitted Deficiencies in Hu et al.

The Office Action relied on no less than three secondary references in an attempt to cure admitted deficiencies in Hu et al. However, Applicants respectfully submit that these reference

[7] Applicants further note that, contrary to the Examiner's assertion, Claim 1 is not a product-by-process claim, reciting titanium disilicide made by a particular process. Rather, Claim 1 recites a "starting structure" with a specific thickness relationship between the titanium layer and the second semiconductor region that can be used to fabricate titanium disilicide. Accordingly, Applicants' argument is not that Claim 1 recites a process for forming titanium disilicide that is different from the one used in Hu et al. Rather, Applicants are asserting that the structure disclosed in Hu et al., which has a low-dose matrix in silicon to modify the grain size in the conductor layer, is different from the "starting structure" recited in Claim 1.

fail to cure the admitted deficiencies, as described below. The following discussion of the secondary references is being presented not to attack the reference individually, but to show that, *when the references are combined*, the combination *as a whole* fails to teach each and every claim element.

a. Wilson et al.

In the Office Action, it was asserted that Figure 16 in Wilson et al. shows that a sheet resistance of less than 3 ohms/square can be achieved for a titanium layer thickness of greater than 500 Angstroms. Applicants note, however, that there is no teaching in Wilson et al. that this sheet resistance can be achieved with line widths no greater than 0.30 μm, as recited in Claim 1. As discussed in Applicants' specification, as line width decreases, it becomes more difficult to achieve a sheet resistance of less than 3 ohms/square. Because Wilson et al. does not teach how this fine line effect can be overcome, it cannot be assumed that the results shown in Figure 16 are achieved for line widths no greater than 0.30 μm.

When Wilson et al. in combined with Hu et al., the semiconductor structure disclosed in Hu et al. is used with the thickness disclosed in Wilson et al. to achieve the results shown in Figure 16. As discussed above, the semiconductor structure used in Hu et al. has a low-dose matrix in silicon to modify the grain size in the conductor layer and is different from the semiconductor structure recited in Claim 1. Accordingly, the addition of Wilson et al. does not cure the deficiency in Hu et al.

Additionally, there is no teaching in Wilson et al. that the titanium layer thickness relates to the thickness of the second semiconductor region in the way recited in Claim 1. The Office Action asserted that there was no apparent dependence on the recited thicknesses of the titanium layer and the second semiconductor region. Applicants respectfully disagree. As discussed at

pages 6-7 of Applicants' specification, Applicants patterned multiple wafers with many titanium disilicide wires and measured the sheet resistance on individual 0.25 μm width lines. Through these measurements, Applicants found that the thickness of the second semiconductor region plays an important role in determining completeness of conversion of the titanium disilicide wires from the C49 phase to the C54 phase. The results of these experiments are shown in Figure 5 of Applicants' specification, and these experiments show that the recited thicknesses are important in avoiding the fine line effect in ensuring that the formed $TiSi_2$ is in ohmic contact with the first semiconductor region and anneals to a phase with a sheet resistance less than 3 ohms/square.

b. Nakayama et al.

In the Office Action, it was asserted that Nakayama et al. discloses low sheet resistance associated with uniform titanium silicide for 0.18 and 0.25 μm lines with no fine line effect. However, Nakayama et al., like Hu et al., does not disclose the semiconductor structure recited in Claim 1. Nakayama et al. teaches that the exposed gate poly-Si edge is effective for improving the fine line effect because Si atoms are easily supplied at the gate edge region and that its semiconductor structure comprises SiN sidewall over-etching with high selectivity to SiO_2. This is different from the semiconductor structure recited in Claim 1. Accordingly, Nakayama et al. does not cure the deficiencies noted above in Hu et al.

In the Office Action, it was asserted that Claim 1 contains product-by-process limitations (the formation of titanium disilicide by a specific process) and that a teaching of the product alone (titanium disilicide) is sufficient to render Claim 1 unpatentable. Applicants respectfully disagree. Claim 1 is not a product-by-process claim — it does not recite titanium disilicide nor does it recite a particular process used to form titanium disilicide. Instead, Claim 1 recites a

semiconductor structure with first and second semiconductor regions and a layer of titanium, with a thickness relationship between the titanium layer and the second semiconductor region. Because Claim 1 is not a product-by-process claim, a teaching of titanium disilicide alone is not sufficient to render the claim unpatentable. Only a teaching of the recited semiconductor structure can render Claim 1 unpatentable, and Nakayama et al. alone or in combination with Hu et al. or the other applied references fails to yield the recited semiconductor structure.

c. Spinelli et al.

Figure 2 in Spinelli et al. was relied upon for the teaching of a typical doping range of silicon over gate oxides. There was no assertion in the Office Action that Spinelli et al. discloses the recited semiconductor structure in Claim 1, and Spinelli et al. does not cure the deficiencies noted above in the other applied references.

4. Conclusion

Because Hu et al. fails to teach the elements asserted to be taught in the Office Action and because the secondary references fail to cure the admitted deficiencies in Hu et al., Applicants respectfully submit that the proposed combination, when viewed as a whole, fails to teach each and every element recited in Claim 1. Accordingly, Applicants respectfully request that the rejections of independent Claim 1 and its dependent claims be removed.

B. Claims 2-6 Are Patentable over the Applied References

Dependent Claims 2-4 recite specific relationships between t1 and t2 that are not shown in the applied references. Claim 2 recites that $t1 \geq 2.2t2$, Claim 3 recites that $t1 = 2.3t2, \pm 0.1t2$, and Claim 4 recites that t1 is about 600Å and t2 is about 250Å. Because none of the applied references teach the importance of these thicknesses with respect to forming $TiSi_2$ without the

"fine line effect," Applicants respectfully submit that there is no suggestion to modify the applied references to yield the claimed invention.

Additionally, Claim 5 recites that the dopant concentration of the first semiconductor region is greater than $1x10^{20}/cm^3$, and Claim 6 recites that the first semiconductor region is doped primarily with boron. Applicants respectfully submit that, because the proposed combination does not teach the first semiconductor region in combination with the other elements recited in Claim 1, one skilled in the art would not have been motivated to use the specific formulations of the semiconductor region recited in dependent Claims 5 and 6. Further, the Office Action provides no reason why one skilled in the art would have been motivated to choose the specific volume concentration recited in Claim 5.

C. Claim 7 Is Patentable over the Applied References

Group II contains independent Claim 7, which recites a semiconductor structure comprising a first semiconductor region characterized by a boron dopant concentration greater than $1x10^{20}/cm^3$ and a set of titanium silicide conductors directly overlying the first semiconductor region and in ohmic contact therewith, with each conductor having a width no greater than 0.3 μm and at least 90% of the conductors characterized by a sheet resistance less than 3 ohms/square. Claim 7 was rejected in view of the same proposed combination used to reject Claim 1. Applicants respectfully submit that, like Claim 1, Claim 7 is patentable over the applied references.

In both the embodiment in Hu et al. that relates to low resistivity, fine-line titanium silicide and in Nakayama et al., there is no teaching of a first semiconductor region characterized by a boron dopant concentration greater than $1x10^{20}/cm^3$. Further, in Wilson et al., there is no disclosure of either the recited boron dopant concentration or the recited line width. Finally,

there is no disclosure of titanium silicide in Spinelli et al. As a result, when the individual references are combined together, the combination, as a whole, fails to teach each and every element recited in independent Claim 7. Accordingly, Applicants respectfully request that the rejections of independent Claim 7.

D. Claim 8 Is Patentable over the Applied References

Group III contains Claim 8, which depends from Claim 1 or 7 and recites that the semiconductor structure comprises a 3-D memory array comprising a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip. In the Office Action, it was admitted that the proposed combination of Hu et al., Wilson et al., Nakayama et al., and Spinelli et al. fails to teach this element. In an attempt to cure this deficiency, it was proposed to add Tsukude et al. to the combination. However, Tsukude et al. merely teaches a stacked-capacitor memory cell. In other words, Tsukude et al. teaches a memory *cell* that has stacked components — not a memory *array* with individual memory cells stacked vertically above one another in a single chip, as recited in Claim 8. Accordingly, even if Tsukude et al. were added to the other references, the proposed combination still fails to yield the claimed invention.

IX. Conclusion

For the reasons set forth above, Applicants respectfully submit that (1) Claims 1-6 are patentable over the proposed combination of Hu et al., Wilson et al., Nakayama et al., and Spinelli et al.; (2) Claim 7 is patentable over the proposed combination of Hu et al., Wilson et al., Nakayama et al., and Spinelli et al.; and (3) Claim 8 is patentable over the proposed combination of Hu et al., Wilson et al., Nakayama et al., Spinelli et al., and Tsukude et al. Accordingly, removal of the rejections is respectfully requested.

Dated: January 21, 2004

Respectfully submitted,

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X. Appendix

1. A semiconductor structure comprising:

a first semiconductor region characterized by a dopant concentration greater than $1x10^{19}/cm^3$;

a second semiconductor region overlying the first semiconductor region, said second semiconductor region comprising silicon and characterized by a dopant concentration less than $1x10^{19}/cm^3$ and a thickness t1; and

a layer comprising titanium directly overlying the second semiconductor region, said layer characterized by a line width no greater than 0.3μm and a thickness t2, wherein $t1 > 1.2t2$;

t1/t2 being sufficiently small that, when the layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide is in ohmic contact with the first semiconductor region;

t1/t2 being sufficiently large that, when the layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide anneals to a phase with a sheet resistance less than 3 ohms/square.

2. The semiconductor structure of Claim 1 wherein $t1 \geq 2.2t2$.

3. The semiconductor structure of Claim 1 wherein $t1 = 2.3t2, \pm 0.1t2$.

4. The semiconductor structure of Claim 1 wherein t1 is about 600Å and t2 is about 250Å.

5. The semiconductor structure of Claim 1 wherein the dopant concentration of the first semiconductor region is greater than $1x10^{20}/cm^3$.

6. The semiconductor structure of Claim 1 or 5 wherein the first semiconductor region is doped primarily with boron.

7. A semiconductor structure comprising:

a first semiconductor region characterized by a boron dopant concentration greater than $1x10^{20}/cm^3$; and

a set of titanium silicide conductors directly overlying the first semiconductor region and in ohmic contact therewith, each said conductor characterized by a width no greater than 0.3μm, and at least 90% of said conductors characterized by a sheet resistance less than 3 ohms/square;

wherein the set of titanium silicide conductors is formed, in part, by a second semiconductor region overlying the first semiconductor region, said second semiconductor region comprising silicon and characterized by a dopant concentration less than $1x10^{18}/cm^3$.

8. The semiconductor structure of Claim 1 or 7 wherein the semiconductor structure comprises a 3-D memory array, wherein the 3-D memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip.

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Joseph F. Hetz - Reg. No. 41,070

Name of Applicant, Assignee or Registered Representative

Signature

Our Case No. 10519-57

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2. Whether Claim 7 is unpatentable under 35 U.S.C. § 103(a) over the proposed combination of Hu et al., Wilson et al., Nakayama et al., and Spinelli et al.; and

3. Whether Claim 8 is unpatentable under 35 U.S.C. § 103(a) over the proposed combination of Hu et al., Wilson et al., Nakayama et al., Spinelli et al., and Tsukude et al.[5]

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[1] U.S. Patent Application No. US 2002/0045342A1.

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A. Claim 1 Is Patentable over the Applied References

1. Introduction

Independent Claim 1 recites a semiconductor structure with first and second semiconductor regions and a titanium layer having a line width no greater than 0.3 μm. Claim 1 also recites a relationship between the thickness of the second semiconductor region and the titanium layer, such that when the titanium layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide is in ohmic contact with the first semiconductor region and anneals to a phase with a sheet resistance less than 3 ohms/square.

In the Office Action, several of the recited claim elements were asserted to be taught by Hu et al. (the primary reference in the 35 U.S.C. § 103(a) rejection), and other recited claim elements were admitted to be missing from Hu et al. Wilson et al., Nakayama et al., and Spinelli et al. were used as secondary references in an attempt to cure the admitted deficiencies. Applicants respectfully submit that independent Claim 1 is patentable over the proposed combination because (1) Hu et al. does not teach the elements asserted in the Office Action to be

present in Hu et al. and (2) the secondary references do not cure the admitted deficiencies in Hu et al.[6]

<u>2. Hu et al. Does Not Teach the Elements Asserted in the Office Action to Be Present in Hu et al.</u>

In the Office Action, it was asserted that element 218 in Figure 2E of Hu et al. is a titanium layer having a line width of less than 0.25 microns. Applicants respectfully disagree. As stated at paragraph 0026 (page 3), element 218 is a conductor layer of tungsten or ***<u>titanium silicide</u>* — *not titanium***. Accordingly, element 218 does not correspond to the layer of titanium recited in Claim 1. Further, the calculated thicknesses in the Office Action were based on the tungsten or titanium silicide layer and do not relate to a thickness of a titanium layer. Accordingly, Hu et al. also fails to disclose the thickness relationship recite in Claim 1.

Additionally, there is no teaching in Hu et al. that element 218 has a line width of less than 0.25 microns, as asserted in the Office Action. There are two disclosed embodiments in Hu et al. One embodiment lowers resistivity by forming a diffusion barrier using oxygen or nitrogen in a word line stack to prevent diffusion from a bottom silicon layer to a conductor layer. ***There is no disclosure in this embodiment of line widths less than 0.3 μm.*** In the second embodiment, barrier elements are used to form a low-dose matrix in silicon to modify the grain size in the conductor layer in order to lower resistivity. It is this embodiment — not the first embodiment — that relates to sub-0.3 micon word lines. However, Figure 2 and the sections of Hu et al. relied upon in the Office Action for the teaching of the titanium layer relate to the first embodiment, which does not teach line widths no greater than 0.3 μm. Accordingly, even if

[6] In the Office Action, the Examiner noted that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. Applicants agree; however, Applicants are not attacking the references individually. The discussion of individual references is presented to show that, *when the references are combined*, the combination *as a whole* fails to teach each and every claim element.

element 218 were a titanium layer, which it is not, Hu et al. would still be deficient because there is no teaching that element 218 has a line width no greater than 0.3 μm, as recited in Claim 1.

Additionally, in the embodiment that relates to sub-0.25 micon word lines, there is no teaching of the semiconductor structure recited in Claim 1. Hu et al. provides a low resistivity, sub-0.25 micon word-line titanium disilicide device by using a semiconductor structure that is different from the one recited in Claim 1. Whereas the semiconductor structure in Claim 1 has a specific thickness relationship between the titanium layer and the second semiconductor region, the semiconductor structure used in Hu et al. does not. Instead, the semiconductor structure used in Hu et al. has barrier elements that form a low-dose matrix in silicon to modify the grain size in the conductor layer. Accordingly, Hu et al. teaches a different semiconductor structure than the one recited in Claim 1.

In summary, because Hu et al. fails to disclose the claim elements asserted to be taught by Hu et al., the foundation of the rejection is fatally flawed. Because the secondary references do not cure this deficiency (or the additional deficiencies admitted by the Examiner), Applicants respectfully submit that Claim 1 is patentable over the proposed combination.[7]

<u>3. The Secondary References Do Not Cure the Admitted Deficiencies in Hu et al.</u>

The Office Action relied on no less than three secondary references in an attempt to cure admitted deficiencies in Hu et al. However, Applicants respectfully submit that these reference

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[7] Applicants further note that, contrary to the Examiner's assertion, Claim 1 is not a product-by-process claim, reciting titanium disilicide made by a particular process. Rather, Claim 1 recites a "starting structure" with a specific thickness relationship between the titanium layer and the second semiconductor region that can be used to fabricate titanium disilicide. Accordingly, Applicants' argument is not that Claim 1 recites a process for forming titanium disilicide that is different from the one used in Hu et al. Rather, Applicants are asserting that the structure disclosed in Hu et al., which has a low-dose matrix in silicon to modify the grain size in the conductor layer, is different from the "starting structure" recited in Claim 1.

fail to cure the admitted deficiencies, as described below. The following discussion of the secondary references is being presented not to attack the reference individually, but to show that, *when the references are combined*, the combination *as a whole* fails to teach each and every claim element.

a. Wilson et al.

In the Office Action, it was asserted that Figure 16 in Wilson et al. shows that a sheet resistance of less than 3 ohms/square can be achieved for a titanium layer thickness of greater than 500 Angstroms. Applicants note, however, that there is no teaching in Wilson et al. that this sheet resistance can be achieved with line widths no greater than 0.30 μm, as recited in Claim 1. As discussed in Applicants' specification, as line width decreases, it becomes more difficult to achieve a sheet resistance of less than 3 ohms/square. Because Wilson et al. does not teach how this fine line effect can be overcome, it cannot be assumed that the results shown in Figure 16 are achieved for line widths no greater than 0.30 μm.

When Wilson et al. in combined with Hu et al., the semiconductor structure disclosed in Hu et al. is used with the thickness disclosed in Wilson et al. to achieve the results shown in Figure 16. As discussed above, the semiconductor structure used in Hu et al. has a low-dose matrix in silicon to modify the grain size in the conductor layer and is different from the semiconductor structure recited in Claim 1. Accordingly, the addition of Wilson et al. does not cure the deficiency in Hu et al.

Additionally, there is no teaching in Wilson et al. that the titanium layer thickness relates to the thickness of the second semiconductor region in the way recited in Claim 1. The Office Action asserted that there was no apparent dependence on the recited thicknesses of the titanium layer and the second semiconductor region. Applicants respectfully disagree. As discussed at

pages 6-7 of Applicants' specification, Applicants patterned multiple wafers with many titanium disilicide wires and measured the sheet resistance on individual 0.25 μm width lines. Through these measurements, Applicants found that the thickness of the second semiconductor region plays an important role in determining completeness of conversion of the titanium disilicide wires from the C49 phase to the C54 phase. The results of these experiments are shown in Figure 5 of Applicants' specification, and these experiments show that the recited thicknesses are important in avoiding the fine line effect in ensuring that the formed $TiSi_2$ is in ohmic contact with the first semiconductor region and anneals to a phase with a sheet resistance less than 3 ohms/square.

b. Nakayama et al.

In the Office Action, it was asserted that Nakayama et al. discloses low sheet resistance associated with uniform titanium silicide for 0.18 and 0.25 μm lines with no fine line effect. However, Nakayama et al., like Hu et al., does not disclose the semiconductor structure recited in Claim 1. Nakayama et al. teaches that the exposed gate poly-Si edge is effective for improving the fine line effect because Si atoms are easily supplied at the gate edge region and that its semiconductor structure comprises SiN sidewall over-etching with high selectivity to SiO_2. This is different from the semiconductor structure recited in Claim 1. Accordingly, Nakayama et al. does not cure the deficiencies noted above in Hu et al.

In the Office Action, it was asserted that Claim 1 contains product-by-process limitations (the formation of titanium disilicide by a specific process) and that a teaching of the product alone (titanium disilicide) is sufficient to render Claim 1 unpatentable. Applicants respectfully disagree. Claim 1 is not a product-by-process claim — it does not recite titanium disilicide nor does it recite a particular process used to form titanium disilicide. Instead, Claim 1 recites a

semiconductor structure with first and second semiconductor regions and a layer of titanium, with a thickness relationship between the titanium layer and the second semiconductor region. Because Claim 1 is not a product-by-process claim, a teaching of titanium disilicide alone is not sufficient to render the claim unpatentable. Only a teaching of the recited semiconductor structure can render Claim 1 unpatentable, and Nakayama et al. alone or in combination with Hu et al. or the other applied references fails to yield the recited semiconductor structure.

c. Spinelli et al.

Figure 2 in Spinelli et al. was relied upon for the teaching of a typical doping range of silicon over gate oxides. There was no assertion in the Office Action that Spinelli et al. discloses the recited semiconductor structure in Claim 1, and Spinelli et al. does not cure the deficiencies noted above in the other applied references.

4. Conclusion

Because Hu et al. fails to teach the elements asserted to be taught in the Office Action and because the secondary references fail to cure the admitted deficiencies in Hu et al., Applicants respectfully submit that the proposed combination, when viewed as a whole, fails to teach each and every element recited in Claim 1. Accordingly, Applicants respectfully request that the rejections of independent Claim 1 and its dependent claims be removed.

B. Claims 2-6 Are Patentable over the Applied References

Dependent Claims 2-4 recite specific relationships between t1 and t2 that are not shown in the applied references. Claim 2 recites that $t1 \geq 2.2t2$, Claim 3 recites that $t1 = 2.3t2, \pm 0.1t2$, and Claim 4 recites that t1 is about 600Å and t2 is about 250Å. Because none of the applied references teach the importance of these thicknesses with respect to forming $TiSi_2$ without the

"fine line effect," Applicants respectfully submit that there is no suggestion to modify the applied references to yield the claimed invention.

Additionally, Claim 5 recites that the dopant concentration of the first semiconductor region is greater than $1x10^{20}/cm^3$, and Claim 6 recites that the first semiconductor region is doped primarily with boron. Applicants respectfully submit that, because the proposed combination does not teach the first semiconductor region in combination with the other elements recited in Claim 1, one skilled in the art would not have been motivated to use the specific formulations of the semiconductor region recited in dependent Claims 5 and 6. Further, the Office Action provides no reason why one skilled in the art would have been motivated to choose the specific volume concentration recited in Claim 5.

C. Claim 7 Is Patentable over the Applied References

Group II contains independent Claim 7, which recites a semiconductor structure comprising a first semiconductor region characterized by a boron dopant concentration greater than $1x10^{20}/cm^3$ and a set of titanium silicide conductors directly overlying the first semiconductor region and in ohmic contact therewith, with each conductor having a width no greater than 0.3 µm and at least 90% of the conductors characterized by a sheet resistance less than 3 ohms/square. Claim 7 was rejected in view of the same proposed combination used to reject Claim 1. Applicants respectfully submit that, like Claim 1, Claim 7 is patentable over the applied references.

In both the embodiment in Hu et al. that relates to low resistivity, fine-line titanium silicide and in Nakayama et al., there is no teaching of a first semiconductor region characterized by a boron dopant concentration greater than $1x10^{20}/cm^3$. Further, in Wilson et al., there is no disclosure of either the recited boron dopant concentration or the recited line width. Finally,

there is no disclosure of titanium silicide in Spinelli et al. As a result, when the individual references are combined together, the combination, as a whole, fails to teach each and every element recited in independent Claim 7. Accordingly, Applicants respectfully request that the rejections of independent Claim 7.

D. Claim 8 Is Patentable over the Applied References

Group III contains Claim 8, which depends from Claim 1 or 7 and recites that the semiconductor structure comprises a 3-D memory array comprising a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip. In the Office Action, it was admitted that the proposed combination of Hu et al., Wilson et al., Nakayama et al., and Spinelli et al. fails to teach this element. In an attempt to cure this deficiency, it was proposed to add Tsukude et al. to the combination. However, Tsukude et al. merely teaches a stacked-capacitor memory cell. In other words, Tsukude et al. teaches a memory *cell* that has stacked components — not a memory *array* with individual memory cells stacked vertically above one another in a single chip, as recited in Claim 8. Accordingly, even if Tsukude et al. were added to the other references, the proposed combination still fails to yield the claimed invention.

IX. Conclusion

For the reasons set forth above, Applicants respectfully submit that (1) Claims 1-6 are patentable over the proposed combination of Hu et al., Wilson et al., Nakayama et al., and Spinelli et al.; (2) Claim 7 is patentable over the proposed combination of Hu et al., Wilson et al., Nakayama et al., and Spinelli et al.; and (3) Claim 8 is patentable over the proposed combination of Hu et al., Wilson et al., Nakayama et al., Spinelli et al., and Tsukude et al. Accordingly, removal of the rejections is respectfully requested.

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X. Appendix

1. A semiconductor structure comprising:

a first semiconductor region characterized by a dopant concentration greater than $1x10^{19}/cm^3$;

a second semiconductor region overlying the first semiconductor region, said second semiconductor region comprising silicon and characterized by a dopant concentration less than $1x10^{19}/cm^3$ and a thickness t1; and

a layer comprising titanium directly overlying the second semiconductor region, said layer characterized by a line width no greater than 0.3μm and a thickness t2, wherein t1 > 1.2t2;

t1/t2 being sufficiently small that, when the layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide is in ohmic contact with the first semiconductor region;

t1/t2 being sufficiently large that, when the layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide anneals to a phase with a sheet resistance less than 3 ohms/square.

2. The semiconductor structure of Claim 1 wherein t1 ≥ 2.2t2.

3. The semiconductor structure of Claim 1 wherein t1 = 2.3t2, ± 0.1t2.

4. The semiconductor structure of Claim 1 wherein t1 is about 600Å and t2 is about 250Å.

5. The semiconductor structure of Claim 1 wherein the dopant concentration of the first semiconductor region is greater than $1x10^{20}/cm^3$.

6. The semiconductor structure of Claim 1 or 5 wherein the first semiconductor region is doped primarily with boron.

7. A semiconductor structure comprising:

a first semiconductor region characterized by a boron dopant concentration greater than $1x10^{20}/cm^3$; and

a set of titanium silicide conductors directly overlying the first semiconductor region and in ohmic contact therewith, each said conductor characterized by a width no greater than 0.3μm, and at least 90% of said conductors characterized by a sheet resistance less than 3 ohms/square;

wherein the set of titanium silicide conductors is formed, in part, by a second semiconductor region overlying the first semiconductor region, said second semiconductor region comprising silicon and characterized by a dopant concentration less than $1x10^{18}/cm^3$.

8. The semiconductor structure of Claim 1 or 7 wherein the semiconductor structure comprises a 3-D memory array, wherein the 3-D memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip.